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Takahisa HIRAIDE:

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For: TESTING APPARATUS AND TESTING METHOD FOR AN INTEGRATED CIRCUIT, AND INTEGRATED CIRCUIT

SUBMISSION OF ENGLISH TRANSLATION

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Attached is the partial English translation of Japanese Patent Application No. 2000-372231, filed December 7, 2000. It is respectfully requested that the attached partial English translation be made of record in the above-identified application

If any further fees are required in connection with the filing of this partial English Translation, please charge same to our Deposit Account No. 19-3935.

Respectfully submitted,

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DECLARATION

I, Setsuko Nakata, residing at 12-16, Sakuragaoka 1-chome, Kugenuma, Fujisawa-shi, Kanagawa 251-0027, Japan, do solemnly and sincerely declare that I well understand both Japanese and English languages and the attached partial English version is a true and faithful translation of the Japanese Application No. 2000-372231 filed on December 7, 2000 in the name of FUJITSU LIMITED.

And I made this solemn declaration conscientiously believing the same to be true.

This 4th day of November , 2005

Setsuko Nakata

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[Document name] Claims

[Claim 2] A testing apparatus for an integrated circuit comprising:

a plurality of shift registers, to which test patterns are inputted, configured with sequential circuit elements inside said integrated circuit;

a mask for masking an indeterminate state in outputs from said plural shift registers and converting the indeterminate state to a specified state; and

an output verifier for verifying output results masked by said mask.

[Claim 3] A testing apparatus for an integrated circuit comprising:

a pattern generator built in said integrated circuit to generate test patterns;

a pattern modifier for modifying said test patterns generated by said pattern generator according to an external input;

a plurality of shift registers configured with sequential circuit elements inside said integrated circuit;

a mask for masking an indeterminate state in outputs from said plural shift registers to which the

test patterns modified by said pattern modifier are inputted, and converting the indeterminate state to a specified state; and

an output verifier for verifying output results masked by said mask.

[Claim 4] The testing apparatus according to claim 2 or 3, wherein said output verifier includes a means for compressing the masked output results.

[Document name] Specification

[Title of the Invention] TESTING APPARATUS AND TESTING METHOD FOR AN INTEGRATED CIRCUIT, AND INTEGRATED CIRCUIT

[0013]

BIST can solve the problems of the above DSPT, but has some problems. Since pseudo random patterns are used in BIST, a quality of the test is in question. In order to increase the fault coverage, it is necessary to apply DSPT as an additional test, or insert such a test point in the internal circuit as to increase controllability and observability. MISR is used to compress data in BIST. However, even once an indeterminate state is captured, all registers in the MISR are brought into the indeterminate state because of the structural nature of the MISR, which makes the test impossible.

[0014]

Since sequential circuit elements including a RAM inside an LSI are generally in the indeterminate state when the power source is turned on, it is necessary to beforehand apply a pattern to initialize these sequential circuit elements, or to invent the circuit such as to prevent the indeterminate state from

propagating to the MISR. Other than this, the designer is forced severe limitations in design when the BIST is applied to an actual circuit in order to prevent a conflict or a float state caused by the random pattern from occurring when a bus and the like is designed, for example. Additionally, inserting the BIST circuit and a test point causes area overhead of the circuit.

[0019]

(2) A testing apparatus according to this invention comprises a plurality of shift registers #0 to #n-1, to which test patterns are inputted, configured with sequential circuit elements inside the integrated circuit, a mask 5 masking an indeterminate state in outputs from the above shift registers #0 to #n-1 and converting the indeterminate state to a specified state, and an output verifier 7a verifying output results masked by the mask 5. Even when results of the sequential circuit elements (internal F/Fs) are compressed and read out to the outside, a result of the compression is not spoiled by the indeterminate state (X state).

[0020]

(3) A testing apparatus according to this

invention comprises a pattern generator 2 built in an integrated circuit to generate test patterns, a pattern modifier 4 modifying the generated test patterns according to an external input, a plurality of shift registers #01 to #n-1 configured with sequential circuit elements inside the integrate circuit, a mask 5 masking an indeterminate state in outputs of the plural shift registers #0 to #n-1, to which the test patterns modified by the pattern modifier 4 are inputted, and converting the indeterminate state to a specified state, and an output verifier 7a verifying the masked output results. Whereby, it becomes possible to increase the number of the scan paths, which permits a shorter time period of the test on the integrated circuit (LSI). It becomes also possible to decrease the amount of data to be stored in the tester because only meaningful data is supplied from the tester (external input) and modified, and to avoid a result of the compression from being spoiled by the indeterminate state.

[0021]

(4) The testing apparatus for an integrated circuit described in the above (2) or (3), the output verifier 7a may include a means for compressing the masked output results, whereby results of the internal F/Fs can be efficiently stored in the output verifier 7a.

[0032]

In the LSI test, it is necessary that values are set to the internal F/Fs through a scan path from the tester, a clock of the system is applied, after that, the value of the internal F/Fs is read out through the scan path and compared with an expected value. When the internal F/Fs are required to operate at a high speed or the number of scan paths is large, BIST employs a method of compressing results of the internal F/Fs and storing them, and afterwards reading them by the tester and comparing them with expected values, not hastily. For this purpose, there is used an MISR configured with an LFSR and an EOR (exclusive OR) gate.

[0033]

According to this invention, it is necessary to compress results of the internal F/Fs and read them out like BIST in order to increase the number of the scan paths. At this time, the indeterminate state (X state) of a RAM or the like might spoil a result of the compression in the MISR as shown in the description of the problems of BIST. An EOR gate is used at an entrance of the MISR, and an EOR gate is also used in a feedback loop of the MISR. If the indeterminate state is present in even one input to the EOR gate, an output

of the EOR gate is brought into the indeterminate state. For this, all registers in the MISR in which an EOR gate is interposed in the feedback loop thereof are degenerated into the indeterminate state. According to this invention, the indeterminate state is masked on the output's side of the scan path.

[0034]

FIG. 3 is a diagram illustrating a testing apparatus according to an embodiment of this invention. In FIG. 3, the testing apparatus comprises a linear feedback shift register (LFSR) 2, a phase shifter 3, a pattern modifier (Pattern Modifying Part) 4, scan paths #0, #1, …, and #n-1, a mask 5, a space compactor 6, and a multiple input signature register (MISR) 7.

[0035]

Pseudo random patterns generated by the LFSR 2 are inputted to the pattern modifier 4 through the phase shifter 3. Control signals from a tester are inputted to the pattern modifier 4 through control input pins or the like. The pattern modifier 4 modifies only a value for an F/F required to be set a value according to the control signals, and inputs and sets the value to the lead F/F of each of the scan paths #0 to #n-1. The mask 5 masks an indeterminate value (X state) among values of the last F/Fs of the scan paths #0 to #n-1 according to the control signal inputted from the control input pin or the like, and

inputs it to the space compactor 6. The space compactor 6 compresses values of the last F/Fs of the scan paths #0 to #n-1 into about the number of bits (for example, 32 bits) of the MISR 7, and inputs them to the MISR 7. The MISR 7 further compresses compressed data from the space compactor 6, and stores it.

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[0048]

FIG. 7 is a diagram illustrating an output verifying part according to the embodiment of this invention. In this example, it is assumed that the MISR 7 is used as the output verifier, and the number of the scan paths is 128. The output verifying part comprises the MISR 7 and the space compactor 6, where outputs of the 128 scan paths #0, #1, …, and #127 are compressed to about the number of bits of the MISR 7 by the space compactor 6, and the compressed data is further compressed by the MISR 7 and stored. To the mask 5, the control signals are inputted through the eight control input pins (b1 to b8). Additionally, outputs of the last F/Fs and outputs of the preceding F/Fs of the last F/Fs on the 128 scan paths #0, #1, …, and #127 are inputted to the mask 5. Outputs of the 128 scan paths are connected to the input side of the last F/Fs on the scan paths, respectively. The

mask 5 controls a shift clock to the MISR 7 (and to LFSR 2) and a shift clock to the F/Fs on the scan paths. When the indeterminate state is masked, only the shift clock for the last F/Fs on the scan paths #0, #1, …, and #127 is applied, whereas the shift clock for other F/Fs on the scan paths and the MISR 7 (and LFSR 2) is suppressed.

[0049]

The mask 5 enables the masking operation at the highest bit (b1) of the control input, and has the decoder circuit 31 to which lower seven bits of the control input are inputted. An indeterminate value (X state value) inputted to a specific one of the 128 scan paths #0, #1, …, and #127 is masked and converted to a "1" state value (or a "0" state value) by the OR circuit (or the AND circuit).

[0050]

Namely, when "1" is inputted to the control input pin b1, an output of the OR circuit 36 becomes "1". Accordingly, the shift clock (negative clock) to F/Fs other than the last F/Fs on the scan paths and the MISR 7 (and the LFSR 2) is suppressed, and the multiplexer 33 is fed back the output of the last F/F according to "1" of the control input pin b1, and outputs it to the OR circuit 32. For this, "1" is outputted from the decoder circuit 31, the indeterminate value (X state value) inputted to a specific one of the 128

scan paths is masked and converted to the "1" state value by the OR circuit 32. When there is also the indeterminate value in an F/F on another scan path at the same time, the indeterminate value from the F/F is masked at the next shift clock.

[0054]

Although a pattern generator (LFSR 2 or the like) used in BIST is used in this invention, such severe design limitations that a specific control circuit for the bus circuit is inserted, a circuit at a test point is inserted for improvement of the detection ration and so forth are not placed on the designer since a deterministic pattern is applied to the inside. A pattern compactor (MISR 7 or the like) used in BIST can be used. Use of the mask 5 can prevent propagation of the indeterminate state inside the circuit to the MISR 7, which can avoid occurrence of a situation where the verification becomes impossible.

[0058]

(2) The indeterminate state in outputs from

the plural shift registers configured with the sequential circuit elements inside the integrated circuit is masked, and a masked output result is verified by the output verifier. Whereby, the indeterminate state (X state) does not spoil a result of compression even if the results from the F/Fs are compressed and read out to the outside.

[0059]

(3) Test patterns generated by the pattern generator built in the integrated circuit are modified by the pattern modifier and inputted to the plural shift registers, the indeterminate state in outputs from the plural shift registers is masked and converted to the specified state, and the masked output result is verified by the output verifier. It is thereby possible to increase the number of the scan paths to shorten the time period of the test on the integrated circuit. It is also possible to decrease the amount of data to be stored in the tester because only meaningful data is supplied from the tester (external input) and modified, and to prevent a result of the compression from being spoiled by the indeterminate state even if results of the internal FFs are compressed and read out to the outside.

[0060]

(4) The output verifier has a means for compressing the masked output result so that the

results of the internal FFs can be efficiently stored in the output verifier.

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